## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A system that mitigates line edge roughness and/or standing wave(s) on pattern lines of a semiconductor device, comprising:

a non-lithographic shrink component that selectively applies heat to a photoresist coating; and

a monitoring component that analyzes the photoresist and controls the application of heat by the non-lithographic shrink component so as to heat the photoresist to a flow point just prior to a melting point of the photoresist to mitigate line edge roughness and/or standing wave(s) on the pattern lines while retaining a target critical dimension.

2. (Original) The system of claim 1, the monitoring component comprising at least one of a scatterometry system and a Scanning Electron Microscopy system.

3. (Original) The system of claim 1, further comprising a processor that processes data associated with at least one of critical dimension, line-edge roughness, and standing wave expression on a photoresist.

4. (Original) The system of claim 3, the processor comprising an artificial intelligence component that facilitates making inferences regarding at least one of mitigating line-edge roughness, mitigating standing wave expression, and achieving target critical dimension on a photoresist.

5. (Original) The system of claim 4, the artificial intelligence component comprising at least one of a support vector machine, a neural network, an expert system, a Bayesian belief network, fuzzy logic, and a data fusion engine.

6. (Original) The system of claim 1, further comprising a memory component that stores data associated with at least one of mitigating line-edge roughness, mitigating standing wave formation and achieving target critical dimension on a photoresist.

7. (Original) The system of claim 6, the memory component comprising at least one of volatile and non-volatile memory.

8. (Original) The system of claim 1, the non-lithographic shrink component comprising at least one of a thermal reflow component, a Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS™) component, and a Shrink Assist Film for Enhanced Resolution (SAFIER) component.

9. (Original) The system of claim 1, further comprising at least one sensor that gathers data associated with at least one parameter of the physical condition of the photoresist.

10. (Currently Amended) A method for mitigating the deleterious effects of an imperfect bottom anti-reflective layer (BARC) on a patterned semiconductor device, comprising:

determining whether at least one of line-edge roughness and standing wave formations are present on patterned photoresist line(s);

employing a non-lithographic shrink technique to heat a photoresist to a glass transition temperature of the photoresist, so that the photoresist begins to exhibit fluid properties, to mitigate extant line-edge roughness and/or standing wave(s); and

retaining critical dimension within a desired tolerance.

11. (Original) The method of claim 10, further comprising processing information associated with photoresist line status.

12. (Original) The method of claim 10, further comprising making inferences regarding photoresist line status.

13. (Original) The method of claim 10, further comprising storing information associated with photoresist line status.

14. (Original) The method of claim 10, the presence of line-edge roughness and/or expressed standing waves is determined *via* employing at least one of a scatterometry technique and Scanning Electron Microscopy.

15. (Original) The method of claim 10, the non-lithographic shrink technique comprising at least one of a thermal reflow technique, a Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS™) technique, and a Shrink Assist Film for Enhanced Resolution (SAFIER) technique.

16. (Original) The method of claim 10, further comprising generating feedback data that facilitates controlling at least one parameter associated with at least one of line-edge roughness mitigation, standing wave mitigation, and critical dimension maintenance.

17. (Currently Amended) A system for mitigating at least one of line-edge roughness and standing wave expression on a patterned semiconductor device, comprising:

means for thermally mitigating line-edge roughness and/or standing wave expression; and

means for maintaining a desired critical dimension during reduction of line-edge roughness and/or standing wave expression.

18. (Original) The system of claim 17, further comprising means for monitoring photoresist line status.

19. (Original) The system of claim 18, the means for monitoring photoresist line status further comprising means for sensing data associated with at least one physical condition of the photoresist.

20. (Original) The system of claim 17, further comprising means for processing information associated with photoresist line status.

21. (Original) The system of claim 17, further comprising means for storing information associated with photoresist line status.

22. (Original) The system of claim 17, further comprising means for making inferences related to photoresist line status.

23. (Original) The system of claim 17, the means for mitigating line-edge roughness and or standing wave expression comprising means for performing a non-lithographic shrink technique.

24. (Original) The system of claim 17, the means for maintaining a desired critical dimension during reduction of line-edge roughness and/or standing wave expression comprising means for temperature regulation.

25. (Original) The system of claim 17, further comprising means for generating feedback data that facilitates controlling at least one parameter associated with at least one of line-edge roughness mitigation, standing wave mitigation, and critical dimension maintenance.